Intel® E8500 Chipset eXternal Memory Bridge (XMB)

Specification Update

March 2005

Notice: The Intel® E8500 chipset eXternal Memory Bridge (XMB) may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 306478-001

Contents

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Revision History

Version	Description	Date
-001	Initial Public Release	March 2005

Preface

This is an update to the specifications in the documents listed in the "Affected Documents" and tables. It is a compilation of device and document errata and specification clarifications/changes, and is intended for hardware system manufacturers and software developers.

Information types defined in the Nomenclature section of this document are consolidated into this document and are no longer published in other documents. This document may also contain previously unpublished information.

Affected Documents

Document Title	Document Number/ Location
Intel® E8500 Chipset Memory Bridge (XMB) Datasheet	306746

Nomenclature

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics,e.g., core speed, L3 cache size, package type, etc. as described in the processor identification information table. Read all notes associated with each S-Spec number.

QDF Number is a several digit code used to distinguish between engineering samples. These samples are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. This document has a processor identification information table that lists these QDF numbers and the corresponding product sample details.

Errata are design defects or errors. These may cause the Short Product Name behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes/Clarifications are modifications to the current published specifications. These changes will be incorporated in the next release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in the next release of the specification.

Note: Errata remain in the specification update throughout the product's life cycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation.

Summary Table of Changes

The tables included in this section indicate the errata, specification changes/ clarifications, or documentation changes that apply to the Intel® E8500 chipset eXternal Memory Bridge (XMB). Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted.

Codes Used in Summary Table

Stepping/Version

X: Applies to this stepping.

Blank: Fixed in listed stepping or does not exist in listed stepping.

Status

No Fix - Root caused to a silicon issue that will not be fixed.

Plan Fix - Root cased to a silicon issue and will be fixed in a future stepping.

Fixed - Root cased to a silicon issue and has been fixed in a subsequent stepping.

Row

Change bar to left of table row indicates that this item is either new or modified from the previous version of this document.

Errata

Number	Stepping	Status	ERRATA
	B-1		
1	X	No Fix	DQS calibration sample data is all 1's
2	X	No Fix	SMBA1 pin drives value after PWRGOOD
3	X	No Fix	Back to back SPD writes cause errors
4	X	No Fix	Pin AA13 (TESTHI) and AA14 (TESTLO) drive values after PWRGOOD.

Specification Changes

Number	SPECIFICATION CHANGES
	There are no Specification Changes in this revision of the Specification Update.

Specification Clarifications

Number	SPECIFICATION CHANGES
	There are no Specification Clarifications in this revision of the Specification Update.

Documentation Changes

Number	DOCUMENTATION CHANGES
	There are no Documentation Changes in this revision of the Specification Update.

Identification Information

Component Identification via Programming Interface

The Intel® E8500 chipset eXternal Memory Bridge (XMB) can be identified by the following register contents:

Stepping	Vendor ID[a]	Device ID[b]	Revision Number[c]
B-1	8086h	2600h	11h

NOTES:

a. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00 - 01h in the PCI function 0 configuration space.

b. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02 - 03h in the PCI function 0 configuration space.

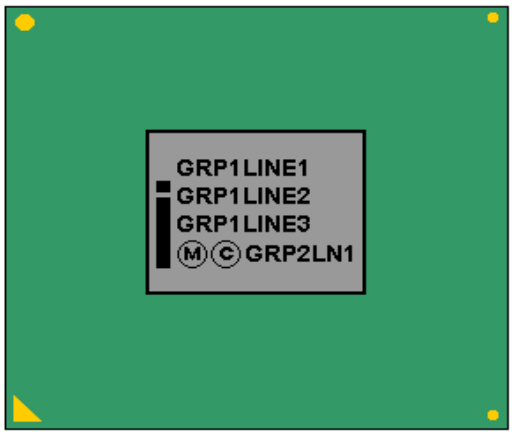
c. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® E8500 chipset eXternal Memory Bridge (XMB) stepping can be identified by the following component markings:

Stepping	QDF-Spec	S-Spec	Top Marking	Notes
B1	QG35	N/A	NQ84001XMB	
B1	TBD	N/A	TBD	Lead Free Package

Figure 1. Top-Side Marking Example (optional)



Errata

All information that has been released in the public document will be removed from the NDA version.

1. DQS calibration sample data is all 1's

Problem: The valid data eye is wider than anticipated in some configurations. In these cases, the DQS sample data from the DCALDATA register measured during the DQS calibration portion of memory initialization may contain all 1's before finding the left edge of the eye.

Implication: This situation makes it impossible to use the data to determine the DQS passband and calibrate the DQS slave delays.

Workaround: The BIOS should set the affected DQSOFCS.DQS offset to 0h. In addition, DRAMISCTL.CH0SLVLEN should be set to 100b for DDR and 011b for DDR2, guaranteeing a sufficient DQS window. The Memory Reference Code revision 0.52 implements this workaround. See the Twin Castle BIOS Specification Update for more details.

Status: There are no plans to fix this erratum.

2. SMBA1 pin drives value after PWRGOOD

Problem: After PWRGOOD is deasserted, the SMBA1 pin may enter a test mode and become an output.

Implication: The XMB latches its SMBus address at PWRGOOD and its operation is unaffected by this issue. Devices which share the SMBA signals with the XMB may sample incorrect values after PWRGOOD is deasserted.

Workaround: PCB designers should isolate the XMB SMBA pins from other signals which rely on the XMB SMBus value.

Status: There are no plans to fix this erratum.

3. Back to back SPD writes cause errors

Problem: The SPD EEPROM spec specifies there should be a 20ms delay between a write transaction and a subsequent read or write. It it possible for the XMB to conduct these transactions faster than this spec.

Implication: SPD writes followed by a subsequent read or write which violate the 20 ms delay window may cause the SPD EEPROM to stop responding. The SPD.SBE (SPD Bus Error) bit will we set.

Workaround: Delays should be inserted into routines which conduct SPD writes to guarantee the 20 ms delay between write transactions and subsequent transactions.

Status: There are no plans to fix this erratum.

4. Pin AA13 (TESTHI) and AA14 (TESTLO) drive values after PWRGOOD.

Problem: After PWRGOOD is deasserted, the AA13 and AA15 pins, listed as inputs, may become outputs and drive values.

Implication: These values are latched during PWRGOOD and are thereafter don’t cares to the XMB. Customers should insure that pull up/down resistors are properly sized to avoid buffer contention with a power plane.

Workaround: None

Status: There are no plans to fix this erratum.

Specification Changes

There are no Specification Changes in this revision of the Specification Update.

Specification Clarifications

There are no Specification Clarifications in this revision of the Specification Update.

Documentation Changes

There are no Documentation Changes in this revision of the Specification Update.

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